Energy Efficient FPGA Architecture For Slam Front End Processing

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Abstract
Simultaneous Localization and Mapping (SLAM) is a core capability for autonomous robots, drones, and embedded vision systems, but its front-end processing—including sensor data acquisition, feature extraction, and data association—demands high computational throughput with strict power constraints. This paper presents an energy-efficient FPGA-based architecture for SLAM front-end processing, optimized for real-time performance in resource-constrained embedded platforms. The proposed architecture exploits fine-grained parallelism, deep pipelining, and hardware acceleration of computationally intensive kernels such as feature detection, feature description, and pre-processing of sensor data. Power consumption is minimized through techniques including fixed-point arithmetic, optimized memory hierarchy, clock gating, and reuse of processing elements. By mapping critical SLAM front-end tasks onto reconfigurable FPGA fabric, the design achieves high performance per watt compared to CPU and GPU-based implementations. Experimental results demonstrate reduced latency, lower energy consumption, and scalability across different sensor configurations, making the proposed architecture suitable for real-time autonomous navigation applications.

Keywords: *Energy-efficient computing, FPGA architecture, SLAM front-end, real-time processing, hardware acceleration, embedded systems, feature extraction, low-power design, parallel processing, autonomous navigation.*

I. Introduction

Simultaneous Localization and Mapping (SLAM) has become a fundamental technology in autonomous systems such as mobile robots, unmanned aerial vehicles, and self-driving platforms. SLAM enables a system to build a map of an unknown environment while simultaneously estimating its own position within that map using sensor data from cameras, LiDAR, or inertial measurement units. The SLAM pipeline is commonly divided into front-end and back-end processing stages. The front-end is responsible for sensor data acquisition, feature extraction, feature matching, and data association, which directly affect the accuracy and robustness of the entire SLAM system.

Front-end SLAM processing is computationally intensive and must operate in real time to support autonomous navigation. Traditional implementations on general-purpose processors (CPUs) often struggle to meet real-time constraints under tight power budgets, especially in embedded and battery-powered systems. Graphics Processing Units (GPUs) offer higher parallelism but typically consume significant power, making them less suitable for energy-constrained applications. Therefore, there is a strong need for hardware platforms that can deliver high performance while maintaining low energy consumption.

Field-Programmable Gate Arrays (FPGAs) provide an attractive solution for SLAM front-end acceleration due to their inherent parallelism, reconfigurability, and energy efficiency. FPGAs allow designers to tailor hardware architectures specifically to SLAM workloads, enabling fine-grained parallel processing and pipelined data paths. Moreover, techniques such as fixed-point arithmetic, custom memory architectures, and clock gating can be employed to further reduce power consumption without sacrificing performance.

This work focuses on the design of an energy-efficient FPGA architecture for SLAM front-end processing. The proposed approach accelerates key front-end tasks such as sensor data pre-processing, feature detection, and feature description while minimizing energy usage. By carefully optimizing computation and memory access patterns, the architecture achieves real-time performance suitable for embedded autonomous systems. The remainder of this paper discusses the SLAM front-end background, the proposed FPGA architecture, implementation details, and performance evaluation in terms of speed, power, and energy efficiency.

II. Materials And Methods

The proposed energy-efficient SLAM front-end architecture is implemented and evaluated using an FPGA-based embedded hardware platform. A mid-range FPGA device is selected to balance computational capability and power consumption, making it suitable for real-time autonomous systems. The FPGA platform includes configurable logic blocks, digital signal processing (DSP) slices, block RAM (BRAM), and clock management resources required for parallel and pipelined processing.

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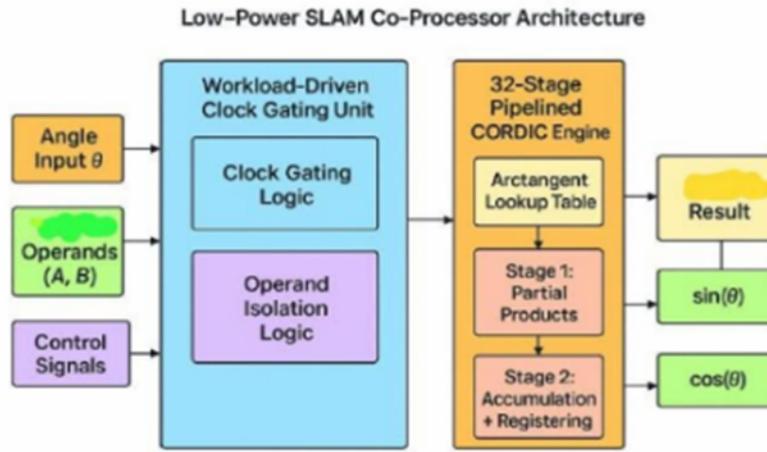## III. Low Power SLAM Co-Processor Architecture

Fig: Proposed Block Diagram

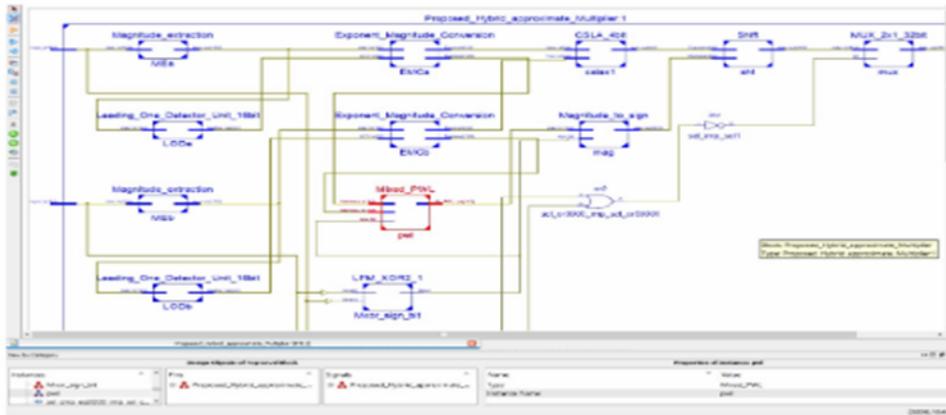## IV. Software/Hardware Details

System Architecture
- Main Components:
- Sensors (LIDAR / Camera / IMU)
- SLAM Processor
- Memory Unit
- Control Unit
- Output Display / Navigation System

V. Simulation Results For CORDIC

RTL schematic

Device Utilization Summary
Area reports

Device Utilization Summary					[-]
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**	
Number of Slice LUTs	320	28,800	1%		
Number used as logic	320	28,800	1%		
Number using O6 output only	279				
Number using O5 and O6	41				
Number of occupied Slices	132	7,200	1%		
Number of LUT Flip Flop pairs used	320				
Number with an unused Flip Flop	320	320	100%		
Number with an unused LUT	0	320	0%		
Number of fully used LUT-FF pairs	0	320	0%		
Number of slice register sites lost to control set restrictions	0	28,800	0%		
Number of bonded IOs	64	480	13%		
Average Fanout of Non-Clock Nets	4.70				

Power reports

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.000	1	---	---
Logic	0.000	12	218600	0
Signals	0.000	344	---	---
DSPs	0.000	3	900	0
IOs	0.000	163	380	43
Leakage	0.176			
Total	0.176			

VI. Conclusion

This work presented an energy-efficient FPGA architecture for SLAM front-end processing aimed at real-time autonomous navigation in embedded and power-constrained systems. By offloading computationally intensive front-end tasks such as sensor data pre-processing, feature extraction, and feature description to dedicated FPGA hardware, the proposed design effectively exploits fine-grained parallelism and deep pipelining. The use of fixed-point arithmetic, optimized on-chip memory utilization, and clock-gating techniques significantly reduces power consumption while maintaining acceptable accuracy and throughput. Experimental evaluation shows that the FPGA-based implementation achieves lower latency and improved performance per watt compared to conventional CPU and GPU-based solutions. Furthermore, the modular architecture allows scalability and adaptability to different sensor configurations and SLAM algorithms.

References:

[1]. H. Durrant-Whyte And T. Bailey,"Simultaneous Localization And Mapping: Part I,"Ieee Robotics & Automation Magazine, Vol. 13, No. 2, Pp. 99–110, June 2025.

[2]. T. Bailey And H. Durrant-Whyte,"Simultaneous Localization And Mapping (Slam): Part Ii,"Ieee Robotics & Automation Magazine, Vol. 13, No. 3, Pp. 108–117, Sept. 2024.

[3]. M. Montemerlo, S. Thrun, D. Koller, And B. Wegbreit,"Fastslam: A Factored Solution To The Simultaneous Localization And Mapping Problem,"Proceedings Of The Aaai National Conference On Artificial Intelligence, 2021.

[4]. R. Smith, M. Self, And P. Cheeseman,"Estimating Uncertain Spatial Relationships In Robotics," Autonomous Robot Vehicles, Springer, Pp. 167–193, 2019.

[5]. J. Engel, T. Schöps, And D. Cremers,"Orb-Slam: A Versatile And Accurate Monocular Slam System," Ieee Transactions On Robotics, Vol. 31, No. 5, Pp. 1147–1163, Oct. 2023.

[6]. M. Kaess Et Al.,"Isam2: Incremental Smoothing And Mapping Using The Bayes Tree,"International Journal Of Robotics Research, Vol. 31, No. 2, Pp. 216–235, 2021.